MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE (UGC – AUTONOMOUS INSTITUTION)

MADANAPALLE – 517325 (A.P)

(Affiliated to JNTUA, Ananthapuramu & Approved by AICTE, New Delhi)

Estd: 1998Registration form for M. Tech (VLSI & Embedded Systems) – I Year II Semester (R24)

(For 2024 admitted batch)

(All the below details are mandatory and should be filled carefully)

Whether the Candidate is appearing for Regular Examinations Supplementary Examination											ons								
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M. Tech

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE – 517325 (A.P.) (UGC – AUTONOMOUS INSTITUTION) Hall

(Affiliated to JNTUA, Ananthapuramu & Approved by AICTE, New Delhi)

Hall Ticket
Duplicate

M. Tech (VLSI & Embedded Systems) – I Year II Semester (R24) (For 2024 admitted batch

M.	Tech

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Tick [$\sqrt{\ }$] the appropriate box to register for a course

1	24VESP103	CMOS Analog IC Design			24VESP410	SoC Architecture
2	24VESP104	Embedded System Design		4	24VESP411	System Design with Embedded Linux
	24VESP407	Pattern Recognition and Machine Learning			24VESP412	Physical Design Automation
3	24VESP408	Programming Languages for Embedded Software		5	24VESP203	CMOS Analog IC Design Laboratory
	24VESP409	RF IC Design		6	24VESP204	Embedded System Design Laboratory
				7	24VESP701	Technical Seminar

Signature of the Candidate	Controller of Examinations

Instructions to Candidates

The candidate has to:

- 1. Display his/her ID card for verification.
- 2. The candidate has to confirm himself/herself that he/she does not possess any foreign material, electronic gadgets other than electronic calculator.
- 3. Candidates should stay in the examination hall at least half-an-hour from the commencement of the examination.
- 4. Be present in the examination hall 15 minutes before the time of commencement of examination. No candidate will be allowed after the commencement of the examination.



MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE – 517325 (A.P) (UGC – AUTONOMOUS INSTITUTION) Hall Ticket

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Original

M. Tech

M. Tech (VLSI & Embedded Systems) – I Year II Semester (R24) (For 2024 admitted batch)

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